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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/565,530	01/23/2006	Teruo Kawabata	070469-0018	9913

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EXAMINER	
YUN, CARINA	
ART UNIT	PAPER NUMBER
2194	
MAIL DATE	DELIVERY MODE
06/01/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/565,530	KAWABATA ET AL.	
	Examiner	Art Unit	
	CARINA YUN	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/17/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's amendments and/or remarks filed on February 23, 2010, claims 10-25 are pending. Claims 1-9 have been cancelled.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 23, 2010 has been entered.

Response to Amendment

3. The 35 U.S.C. 112 rejections to claim 1-25 has been withdrawn in light of the amendments made to the claims.

Information Disclosure Statement

4. The information disclosure statement filed May 17, 2010 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the reference Japanese Office Action dated 2/16/2010 is not in English language. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Drawings

5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. Claim 23 is objected because it is dependent on claim 1 which is now cancelled. Applicant is advised to cancel this claim or change it to depend on a pending claim. For the interest of compact prosecution, examiner is interpreting claim 23 to depend on claim 10.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 10, 17, 18, and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Chang (U.S. Pat. No. 5,805,863).

Regarding claim 10, Hobbs teaches a program conversion device for a processor which has an instruction set including an instruction that waits for a predetermined response from an outside source when the instruction is executed (see Fig. 1 and also ¶ [0020] and ¶ [0021] describing the device (e.g. computer) used to perform the compilation procedures), the device comprising: a CPU (see scalar processor ¶ [0024] and Fig. 3, 200); and a compiler system including (see ¶ [0020] compiler): a loop structure transforming unit operable to perform double looping transformation so as to transform a structure of a loop (see double loop structure, see ¶ [0047]), which is included in an input program and whose iteration count is x, into a nested structure where a loop whose iteration count is y is an inner loop and a loop whose iteration count is x/y is an outer loop (see nested loop structure, ¶ [0047]); and an instruction placing unit configured to convert the input program into an output program including the instruction by

placing the instruction in a position outside the inner loop (see abstract and prefetch instruction outside inner loop, see ¶ [0051] and ¶ [0052]).

Hobbs does not specifically disclose wherein the loop structure transforming unit is further configured to split off, from the loop whose iteration count is x, the loop whose iteration count is y, where y = (cache line size) / {size of an array referenced within the loop whose iteration count is x) × (a value of an increment of the array)}.

However, Chang teaches wherein the loop structure transforming unit is further configured to split off, from the loop whose iteration count is x, the loop whose iteration count is y (see col. 5, lines 43-53, which describe optimization techniques such as loop transformation), where y = (cache line size) / {size of an array referenced within the loop whose iteration count is x) × (a value of an increment of the array)} ("y.sub.-- stride" is the change in memory address per outer loop iteration, divided by the reference size. As with X.sub.-- stride, the reference size is the number of bytes of memory occupied by the reference, which depends upon the data type of the reference. Dividing by the reference size puts x.sub.-- stride in terms of array elements, as opposed to memory address space, see col. 5, lines 10-18). Hence it would have been obvious to modify the teachings of Hobbs by adapting the teachings of Chang in order to further optimize loop transformation.

Regarding claim 17, Hobbs teaches that when an execution count of a loop is non-fixed, the loop structure transforming unit is operable to judge the execution count of the loop when the loop is executed and to perform double looping transformation so as to dynamically vary an iteration count in accordance with a judgment result (see ¶ [0052-0053]; Examiner notes the code segment shows the variable loop, the double looping transformation).

Regarding claim 18, Hobbs teaches further comprising a receiving unit operable to receive information showing that arrays are aligned to a cache line size, that the instruction placing unit is operable to place a prefetch instruction in the loop, whose iteration count is x, for prefetching data stored one cache line ahead of data to be referenced within the iteration processing of the loop that is executed x number of times (i.e. loop optimization with prefetch, relating to size of cache memory is described. see ¶[0040] and ¶[0041]).

Regarding claim 20, Hobbs teaches that when the arrays are not aligned to the cache line size, the instruction placing unit is operable to place a prefetch instruction in the loop, whose iteration count is x, for prefetching data stored two cache lines ahead of data to be referenced within the iteration processing of the loop that is executed x number of times (i.e. loop optimization with prefetch, relating to size of cache memory is described. see ¶[0040] and ¶[0041]).

Regarding claim 21, Hobbs teaches that when the arrays are not aligned to the cache line size, the loop structure transforming unit is operable to judge a relative position in a cache line, from which the array starts to access, and operable to perform double looping transformation in accordance with a judgment result (see ¶ [0040]).

Regarding claim 22, Hobbs teaches further comprising a receiving unit operable to receive information that relates to a focused array (i.e. arrays that are allocated, see ¶ [0032]), that the loop structure transforming unit is operable to perform double looping transformation only on the focused array (i.e. loop restructuring, see ¶ [0033]).

Regarding claim 23, Hobbs teaches that the loop structure transforming unit is operable to further perform double looping transformation on an outer loop, considering an innermost

loop as one block (see ¶ [0039] describing that the loop may be transformed into separate loops with inner and outer loops, see ¶ [0047] showing example of double loop transformation).

Regarding claims 24 and 25, are method claims corresponding to independent claim 10, above. Therefore, these claims are rejected for the same reasons as indicated for claim 10.

10. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Chang (U.S. Pat. No. 5,805,863) as applied to claim 10, further in view of Nishiyama (U.S. Pat No. 6,148,439).

Regarding claim 11, Hobbs and Chang do not specifically disclose that when a plurality of arrays are present, the loop structure transforming unit is operable to further perform, in accordance with the number of the arrays, proportional dividing transformation to proportionally divide the loop whose iteration count is y and on which the double looping transformation has been performed. However, Nishiyama teaches that when a plurality of arrays are present, the loop structure transforming unit is operable to further perform, in accordance with the number of the arrays, proportional dividing transformation to proportionally divide the loop whose iteration count is y and on which the double looping transformation has been performed (see Fig. 15, Examiner notes a plurality of arrays are shown in the drawing, the loop is proportionally divided, see also col. 3, lines 35-45). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Chang to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs teachings of loop optimization for better performance.

Regarding claim 12, Hobbs and Chang do not specifically disclose that when sizes of array elements of the plurality of arrays are different, the loop whose iteration count is y is

proportionally divided in the proportional dividing transformation in accordance with a ratio of the sizes. However, Nishiyama teaches that when sizes of array elements of the plurality of arrays are different, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the sizes (see col. 3, lines 30-35). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Chang to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs teachings of loop optimization for better performance.

Regarding claim 13, Hobbs and Chang do not specifically disclose that when each stride of the plurality of arrays is different, a stride referring to addresses advanced per set of the iteration processing of the loop, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the strides. However, Nishiyama teaches that when each stride of the plurality of arrays is different, a stride referring to addresses advanced per set of the iteration processing of the loop, the loop whose iteration count is y is proportionally divided in the proportional dividing transformation in accordance with a ratio of the strides (see Fig. 15 and col. 3, lines 30-35; Examiner notes the arrays are different sizes, see 1501, 1502, and are proportionally divided). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Chang to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs teachings of loop optimization for better performance.

Regarding claim 14, Hobbs and Chang do not specifically disclose that when an inner loop is transformed, a conditional statement is generated for each divided loop and the proportional dividing transformation is performed so that each divided loop is executed within a same inner loop. However, Nishiyama teaches that when an inner loop is transformed, a conditional statement is generated for each divided loop and the proportional dividing transformation is performed so that each divided loop is executed within a same inner loop (see Fig. 3B, conditional IF statement). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to further combine the teachings of Hobbs and Chang to include loop splitting because Nishiyama teaching regarding loop splitting would optimize Hobbs teachings of loop optimization for better performance.

11. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs (U.S. 2002/0199178 A1) in view of Chang (U.S. Pat. No. 5,805,863) as applied to claim 10, further in view of Liu (U.S. Pat No. 6,070,011).

Regarding claim 15, Hobbs and Chang do not specifically disclose that when the loop whose iteration count is y is split off from the loop whose iteration count is x and a remainder z left over after a calculation of x/y is not zero, the loop structure transforming unit is operable to perform peeling processing and then double looping transformation on iteration processing that is to be executed z number of times. However, Liu teaches that when the loop whose iteration count is y is split off from the loop whose iteration count is x and a remainder z left over after a calculation of x/y is not zero, the loop structure transforming unit is operable to perform peeling processing and then double looping transformation on iteration processing that is to be executed z number of times (i.e. loop peeling technique used with conditional, see col. 4, lines 37-49).

Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hobbs, Chang, and Liu because Liu teaching of loop peeling would improve the loop optimization technique for better performance.

Regarding claim 16, Hobbs and Chang do not specifically disclose that when the remainder z is not zero, the loop structure transforming unit is operable to generate a conditional statement for judging whether a loop count of an inner loop is y or z and to perform double looping transformation. However, Liu teaches that when the remainder z is not zero, the loop structure transforming unit is operable to generate a conditional statement for judging whether a loop count of an inner loop is y or z and to perform double looping transformation (see code segment described in col. 7, lines 6-35; Examiner notes IF/ELSE conditional statement is shown, along with looping transformation). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hobbs, Chang, and Liu because Liu's teaching of loop peeling would improve the loop optimization technique for better performance.

12. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hobbs et al. (U.S. 2002/0199178 A1) in view of Chang (U.S. Pat. No. 5,805,863) as applied to claim 10, and further in view of Ogawa et al. (U.S. Pub No. 2004/0098713 A1).

Regarding claim 19, Hobbs teaches the loop structure transforming unit is operable to perform the double looping transformation in accordance with the information (see double looping transformation, ¶ [0047]). It is noted that Hobbs and Chang do not specifically disclose that the optimization directive information receiving unit is operable to receive information showing a relative position in a cache line, from which the array starts to access. However,

Ogawa teaches that the optimization directive information receiving unit is operable to receive information showing a relative position in a cache line, from which the array starts to access (i.e. the compiler according to the present invention receives a directive on alignment for allocating array data to the memory region and performs optimization following the directive, see ¶ [0020]). Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Hobbs, Chang, Ogawa because Ogawa's teaching of optimization directive information would improve the optimization technique used for loop optimization for better performance.

Response to Arguments

13. Applicant's arguments with respect to claims 10-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CARINA YUN whose telephone number is (571)270-7848. The examiner can normally be reached on Mon-Thur, 9.30am-6.30pm; alt. Fri, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, SAM SOUGH can be reached on (571)272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C. Y./
Examiner, Art Unit 2194

/Hyung S. Sough/
Supervisory Patent Examiner, Art Unit 2194
May 27, 2010